

Amendments to the Drawings

Figures 1, 2, 3, and 12 have been amended to add the word “prior art.”

Attachment: Replacement Sheet

Annotated Marked-Up Drawings

**REMARKS**

As requested, Figures 1-3 have been labeled as “prior art.” Figure 12 has also been so labeled. Figure 4 is not considered to be prior art.

All claims have been rejected under 35 U.S.C. 102 or 103 as being unpatentable over Pulvirenti, et al. (6,791,212), alone or in combination with Wada, et al. (6,403,943). That rejection is respectfully traversed and reconsideration is requested. Further, each independent claim has been amended to further distinguish the cited references.

As discussed, for example, at pages 5 and 6 of the specification, the present invention deals with a problem of noise that results with current peaks during switch transitions in a charge pump circuit. In accordance with the invention, the current through the charge pumping capacitance during those switch transitions is limited by a resistance. However, at certain operating points, that resistance should be reduced or eliminated. Thus, in accordance with the claims, a variable resistance is provided and that variable resistance is varied with operating point.

The Pulvirenti circuit includes a charge pumping circuit illustrated in Fig. 4. It includes an input current at terminal 4a and a pumping capacitor at 28. Relative to the claimed variable resistance with varied operating point, the Examiner has referred to resistance 18 described at column 3, lines 24-31. As there described, the variable resistance 18 programs “the steady-state condition value of the boosted voltage  $V_{LCD}$ .” Thus, the variable resistance controls, through a feedback loop, the steady-state output voltage to which the charge pump circuit pumps. However, as can be seen by the combination of figures 2 and 4, the resistance 18 would not limit current spikes through the pumping capacitor  $C_p$  during switch transitions. Rather, by providing feedback to the error amplifier 14 and oscillator 15, it would only control the times at which those transitions occurred.

Each claim recites that the resistance is varied with varied operating point. The resistance 18 of Pulvirenti is not varied with varied operating point; rather, it controls the output voltage. Nonetheless, the claims have been amended to more explicitly recite the operation of the variable resistance relative to the charge pumping capacitance of the circuit. There is no suggestion in Pulvirenti, et al. of a variable resistance “to limit noise generating current spikes

through the pumping capacitance during switch transitions.” Accordingly, all claims should be allowed.

The showing of a variable resistance in Wada does not overcome the above deficiencies of Pulvirenti. Wada does not relate to a charge pumping circuit.

### CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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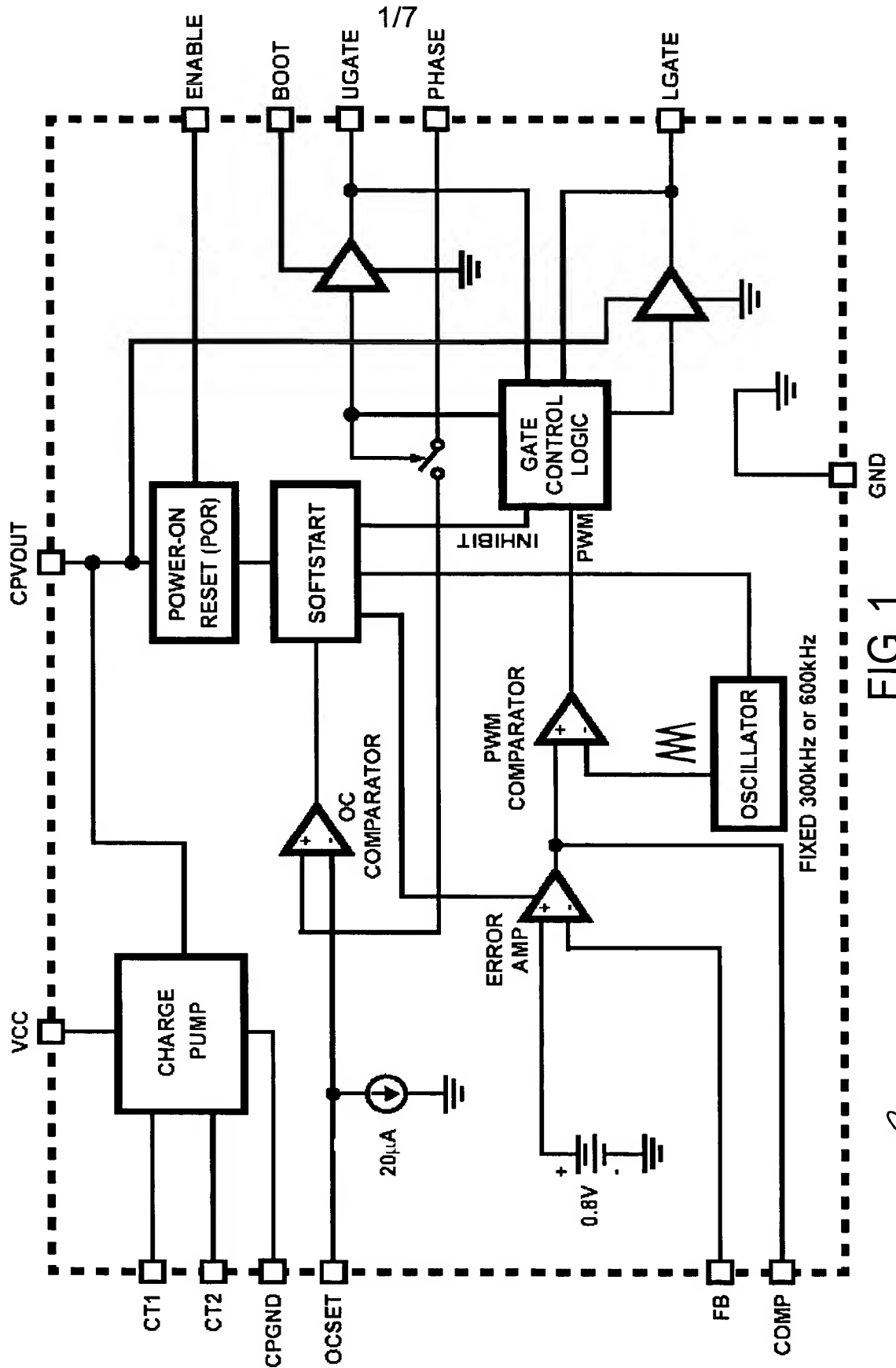


FIG. 1

*Prior Art*

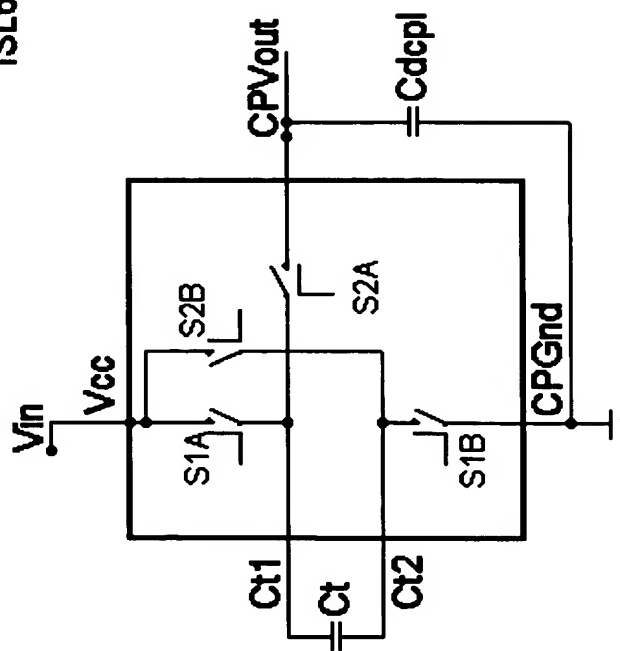


FIG. 3

The diagram illustrates the proposed buck DCDC converter architecture. It features an **Internal Charge Pump** and **PWM Control** block, which is powered by  $V_{in}$  and  $V_{cc}$ . The internal charge pump's output,  $CPV_{out}$ , is connected to the **External Charge Pump** block, which consists of a diode  $D1$ , a diode  $D2$ , and a capacitor  $C24$ . The output of the external charge pump is connected to the **Buck DCDC Converter Power Stage**, which includes a MOSFET  $Q6$ , a MOSFET  $Q7$ , an inductor  $L1$ , and a capacitor  $C_o$ . The output of the buck converter is  $V_{out}$ . A **Noise Reducing Control** block is connected to the  $V_{in}$  and  $V_{out}$  lines, and its output is connected to the **PWM Control** block. The **PWM Control** block also receives feedback from the  $V_{out}$  line through a capacitor  $C_{dcpl}$ . The **Internal Charge Pump** block is connected to the  $V_{in}$  and  $V_{cc}$  lines, and its output is connected to the  $V_{out}$  line through a capacitor  $C_{t1}$  and a resistor  $R_{t1}$ . The **Internal Charge Pump** block is also connected to the  $V_{cc}$  line through a capacitor  $C_{t2}$  and a resistor  $R_{t2}$ .

FIG. 13